

AMENDMENTS TO THE CLAIMS

1 1. (Canceled)

1 2. (Canceled)

1 3. (Canceled)

1 4. (Currently Amended) A memory system, comprising:
2 a memory cell;
3 first and second bitlines operably connected to said memory cell;
4 a write line operably connected to said memory cell; and
5 an equilibration circuit controlled by a reference voltage, said equilibrium circuit
6 connected to said first and second bitlines, said equilibrium circuit
7 comprising first and second pMOS devices in series with said first and
8 second bitlines, respectively, and a third pMOS device connected between
9 said first and second bitlines and wherein the gates of said first, second
10 and third pMOS devices are connected to said reference voltage, [[.]]
11 wherein said first, second and third pMOS devices operate as resistors in
12 the linear region of MOSFET device operation, and wherein said
13 equilibration circuit is operable:
14 to maintain a predetermined equilibrium condition between said first
15 and second bit lines; and
16 to generate an impedance load in said first and second bit lines at a
17 level that allows generation of differential signals in said bit
18 lines.

1 5. (Original) The memory system according to claim 4, wherein the
2 resistance of said first, second and third pMOS devices is determined by the gate-source
3 voltage of said pMOS devices.

1 6. (Original) The memory system according to claim 5, wherein said
2 write line is operably connected to said memory cell by at least one transfer gate.

1 7. (Original) The memory system according to claim 6, wherein said
2 transfer gate comprises an nMOS device and wherein said reference voltage is related to
3 the gate drive current of said transfer gate.

1 8. (Original) The memory system according to claim 7, wherein said
2 reference voltage is controlled by a reference circuit that is operable to change said
3 reference voltage to compensate for variations in operating characteristics of said first,
4 second and third pMOS devices.

1 9. (Original) The memory system according to claim 8, wherein said
2 reference circuit is further operable to change the reference voltage to compensate for
3 variations in the operating characteristics of said nMOS device comprising said transfer
4 gate.

1 10. (Original) The memory system according to claim 9, wherein said
2 reference circuit comprises a current mirror.

1 11. (Canceled)

1 12. (Canceled)

1 13. (Canceled)

1 14. (Currently Amended) A method for controlling operation of a memory
2 system, comprising:
3 storing information in a memory cell;
4 generating a predetermined equilibrium condition between first and second
5 bitlines operably connected to said memory cell using an equilibration
6 circuit connected to said first and second bitlines, said equilibrium circuit
7 being controlled by a reference voltage and comprising first and second
8 pMOS devices in series with said first and second bitlines, respectively,
9 and a third pMOS device connected between said first and second bitlines,
10 wherein the gates of said first, second and third pMOS devices are
11 connected to said reference voltage and, [[,]] wherein said first, second

12 and third pMOS devices operate as resistors in the linear region of
13 MOSFET device operation; and
14 controlling the content of information in said memory cell with a write line
15 operably connected to said memory cell.

1 15. (Original) The method according to claim 14, wherein the resistance
2 of said first, second and third pMOS devices is determined by the gate-source voltage of
3 said pMOS devices.

1 16. (Original) The method according to claim 15, wherein said write line
2 is operably connected to said memory cell by at least one transfer gate.

1 17. (Original) The method according to claim 16, wherein said transfer
2 gate comprises an nMOS device and wherein said reference voltage is related to the gate
3 drive current of said transfer gate.

1 18. (Original) The method according to claim 17, wherein said reference
2 voltage is controlled by a reference circuit that is operable to change said reference
3 voltage to compensate for variations in operating characteristics of said first, second and
4 third pMOS devices.

1 19. (Original) The method according to claim 18, wherein said reference
2 circuit is further operable to change the reference voltage to compensate for variations in
3 the operating characteristics of said nMOS device comprising said transfer gate.

1 20. (Original) The method according to claim 19, wherein said reference
2 circuit comprises a current mirror.

1 21. (Canceled)

1 22. (Canceled)

1 23. (Canceled)

1 24. (Currently Amended) A digital processing system, comprising:
2 a datapath module;
3 a control module;
4 an input-output module; and
5 a memory cell;
6 first and second bitlines operably connected to said memory cell;
7 a write line operably connected to said memory cell; and
8 an equilibration circuit controlled by a reference voltage, said equilibrium circuit
9 connected to said first and second bitlines, said equilibrium circuit
10 comprising first and second pMOS devices in series with said first and
11 second bitlines, respectively, and a third pMOS device connected between
12 said first and second bitlines and wherein the gates of said first, second
13 and third pMOS devices are connected to said reference voltage, [[.]]
14 wherein said first, second and third pMOS devices operate as resistors in
15 the linear region of MOSFET device operation, wherein said equilibration
16 circuit is operable:
17 to maintain a predetermined equilibrium condition between said first
18 and second bit lines; and
19 to generate an impedance load in said first and second bit lines at a
20 level that allows generation of differential signals in said bit
21 lines.

1 25. (Previously Presented) The digital processing system according to
2 claim 24, wherein the resistance of said first, second and third pMOS devices is
3 determined by the gate-source voltage of said pMOS devices.

1 26. (Previously Presented) The digital processing system according to
2 claim 25, wherein said write line is operably connected to said memory cell by at least
3 one transfer gate.

1 27. (Previously Presented) The digital processing system according to
2 claim 26, wherein said transfer gate comprises an nMOS device and wherein said
3 reference voltage is related to the gate drive current of said transfer gate.

1 28. (Previously Presented) The digital processing system according to
2 claim 27, wherein said reference voltage is controlled by a reference circuit that is
3 operable to change said reference voltage to compensate for variations in operating
4 characteristics of said first, second and third pMOS devices.

1 29. (Previously Presented) The digital processing system according to
2 claim 28, wherein said reference circuit is further operable to change the reference
3 voltage to compensate for variations in the operating characteristics of said nMOS device
4 comprising said transfer gate.

1 30. (Previously Presented) The digital processing system according to
2 claim 29, wherein said reference circuit comprises a current mirror.